REMARKS

Claims 1-37 are all the claims presently pending in the application.

Applicants gratefully acknowledge that **claims 4, 10, 11, 14, 17, 19, 23-26, 28, and 30-37** would be **allowable** if rewritten in independent form.

Applicants note that claim 13 recites somewhat similar subject matter as the Examiner's reasons for allowance, and also has not been rejected on prior art grounds. Thus, **claim 13** also should be **allowable**.

Applicants also note that claim 18 has not been rejected on prior art grounds or indicated as containing allowable subject matter.

Applicants respectfully submit, however, that all of the claims are allowable, for the following reasons. Applicants reserve the right to rewrite **allowable claims 4, 10, 11, 13, 14, 17, 19, 23-26, 28, and 30-37** in independent form at a later time.

While Applicants believe that all of the claims are in condition for immediate allowance, to speed prosecution, claims 1, 8, 15, 27, and 29 have been amended to define more clearly and particularly the features of the claimed invention.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claim 27 stands rejected upon informalities (e.g., 35 U.S.C. § 112, first paragraph).

With respect to the prior art rejections, claims 1-3, 5, 6, and 29 stand rejected under 35 U.S.C. §102(b) as being anticipated by Tsukamoto, et al. (U.S. Patent No. 4,931,897). Claims 1,

3, 6-8, 12, and 20-22 stand rejected under 35 U.S.C. §102(b) as being anticipated by Anjum, et al. (U.S. Patent No. 5,429,972). Claims 1, 3, 6-8, 15, and 16 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Pourkeramati (U.S. Patent No. 5,953,254). Claims 1, 3, 6, 7, 9, and 12 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Niroomand, et al. (U.S. Patent No. 6,228,740).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The present invention relates to a semiconductor device and method therefor, and more particularly, to a structure and method of ultra-small nano-scale (e.g., within a range of about 10 nm to about 20 nm) grain size polysilicon.

In the related art, complementary metal oxide semiconductor (CMOS) gates are beginning to target 30 nm lengths. On the other hand, typical polysilicon grain sizes are in the 50 nm range which creates many problems including that the polysilicon is more bamboo-like along the gate lines, and conductivity/resistivity becomes more sensitive to grain size at this nano-scale level (e.g., conductivity/resistivity tracks with grain size). Another problem is that the diffusion of dopants in these "large-grain" polysilicon gates will probably be mostly through lattice diffusion (similar to that of crystalline silicon) which is relatively slow (e.g., typically about a factor of 10 slower than diffusion for polysilicon) and sufficient dopant may not reach the polysilicon/oxide interface, where dopant is also needed to prevent polysilicon depletion effects.

Therefore, for small gate lengths, it is very useful to have polysilicon with a much smaller average grain size of 10-20 nm. However, it is well known that polycrystalline grain size

may somewhat correlate with film thickness, and given that the typical gate stack thicknesses are in the 100 nm range, it is difficult to limit the grain size to the 10-20 nm range. The related art methods at controlling the average grain size through various deposition conditions have consistently yielded best defect-free material only in the ~50 nm average grain size range.

The claimed invention, on the other hand, provides a method for making small nano-scale grained polysilicon with a concomitant structure that results therefrom. With the unique and unobvious aspects of the present invention, ultra-small polysilicon grains at nano-scale size (e.g., within a range of about 10 nm to about 20 nm) can be created, and their size can be retained through heat cycles.

For example, the claimed invention advantageously breaks the polysilicon film into two parts where the first layer sets the polysilicon grain size.

As exemplarily defined by independent claim 1, a method of forming a semiconductor structure, includes providing a nitride layer between a silicon-containing layer and a polysilicon layer, wherein the silicon-containing layer includes a grain size substantially within a nano-scale size.

The present inventors have recognized that breaking the polysilicon film into two parts (e.g., first and second layers) where the first polysilicon layer sets the polysilicon grain size, is very advantageous in achieving such ultra small polysilicon grain size. Then, the remaining polysilicon (e.g., second layer of polysilicon) is grown (deposited) on the nitride barrier to set the correct gate stack thickness.

Thus, the claimed invention advantageously is easily and inexpensively integrated into the process and is applicable to any substrate, bulk or silicon-on-insulator (SOI), SiGe, etc.

Additionally, the claimed invention provides a small grain size which facilitates dopant diffusion and reduces polysilicon depletion.

II. THE 35 U.S.C. §112, FIRST PARAGRAPH REJECTION

Claim 27 stands rejected under 35 U.S.C. §112, first paragraph, as allegedly failing to comply with the enablement requirement.

Applicants respectfully submit, however, that one of ordinary skill in the art could practice (e.g., make and use) the invention (e.g., the claimed invention as exemplarily defined by claim 27), without undue experimentation.

For example, the specification clearly explains that the present inventors have recognized that breaking the polysilicon film into two parts (e.g., first and second layers) where the first polysilicon layer sets the polysilicon grain size, is very advantageous in achieving such ultra small polysilicon grain size (e.g., see specification at page 4, lines 21-24; page 6, lines 14-15).

That is, the specification clearly explains, with reference to the exemplary aspects of the invention, that the silicon-containing layer a-Si (e.g., 120) will convert to polysilicon (e.g., 125) with about 10-20 nm grain size (e.g., see Figure 2, reference numeral 125 which illustrates the small grain (about 10-20 nm grain size) polysilicon layer; e.g., the first polysilicon layer)(e.g., see specification at page 8, lines 11-13).

Then, the remaining polysilicon (e.g., second layer of polysilicon; see Figure 3, reference numeral 140) is grown (deposited) on the nitride barrier (e.g., 130) to set the correct gate stack thickness. The grain size of the polysilicon layer 140 (e.g., the second polysilicon layer), however, can be different (e.g., typically within a range of about 30 nm to about 80 nm), while

the polysilicon layer 125 retains its small grain size because of the ultra-thin nitride barrier (e.g., see specification at page 8, lines 11-17).

The specification further notes that there is no limit to the thickness of the polysilicon 140 (e.g., the second polysilicon layer) which is deposited, but typically it is within a range of about 80 nm to about 130 nm. The typical gate stack generally has a height (thickness) of about 100-150 nm (e.g., see specification at page 8, lines 18-24).

Thus, Applicants submit that one of ordinary skill in the art could practice (e.g., make and use) the invention (e.g., the claimed invention as exemplarily defined by claim 27), without undue experimentation.

While Applicants believe that claim 27 is patentable over the cited references, to speed prosecution, claim 27 has been amended to define more clearly and particularly that the gate stack includes a silicon-containing layer and a polysilicon layer with a nitride layer therebetween, wherein a grain size of the silicon-containing layer is set without affecting a polysilicon grain size of the polysilicon layer, thereby reciting somewhat similar features as those set forth by the Examiner in the "Statement of Reasons for Allowance" (see Office Action at page 7, second paragraph). Thus, claim 27 also should be in condition for immediate allowance.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. THE PRIOR ART REJECTIONS

Claims 1-3, 5, 6, and 29 stand rejected under 35 U.S.C. §102(b) as being anticipated by Tsukamoto. Claims 1, 3, 6-8, 12, and 20-22 stand rejected under 35 U.S.C. §102(b) as being

anticipated by Anjum. Claims 1, 3, 6-8, 15, and 16 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Pourkeramati. Claims 1, 3, 6, 7, 9, and 12 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Niroomand.

While Applicants believe that claims 1-3, 5-9, 12, 15, 16, 20-22, and 29 are patentable over the cited references, to speed prosecution, claims 1, 8, 15, and 29 have been amended to define more clearly and particularly the features of the claimed invention.

For example, independent claim 1 is amended to define more clearly and particularly that "*said silicon-containing layer has a grain size substantially within a nano-scale size*" (emphasis added) as described, for example, in the specification at page 4, lines 6-9, and page 6, lines 11-13).

Thus, Applicants submit that none of the cited references discloses or suggests at least these features of independent claim 1. Therefore, independent claim 1 is not anticipated by (or for that matter, rendered obvious from) Tsukamoto, Anjum, Pourkeramati, or Niroomand at least for somewhat similar reasons as the Examiner's "Statement of Reasons for Allowance".

On the other hand, dependent claims 8 and 15 are amended to include somewhat similar features as claim 5, thereby reciting somewhat similar combinations of features as those set forth by the Examiner in the "Statement of Reasons for Allowance" (see Office Action at page 7, second paragraph). Thus, claims 8 and 15 also should be in condition for immediate allowance.

Independent claim 29 is amended to define more clearly and particularly that "*said grain size of said first polysilicon layer has a grain size substantially within a nano-scale size*" (emphasis added) as described, for example, in the specification at page 4, lines 6-9, and page 6, lines 11-13).

Thus, Applicants submit that none of the cited references discloses or suggests at least these features of independent claim 29. Therefore, independent claim 29 is not anticipated by (or for that matter, rendered obvious from) Tsukamoto, Anjum, Pourkeramati, or Niroomand at least for somewhat similar reasons as the Examiner's "Statement of Reasons for Allowance".

For the foregoing reasons, Applicants respectfully submit that claims 1-3, 5-9, 12, 15, 16, 20-22, and 29 are not anticipated by Tsukamoto, Anjum, Pourkeramati, or Niroomand.

IV. FORMAL MATTERS

A. The Office Action objects to the specification for allegedly deeming an ultra-thin silicon nitride layer as being "*known to be electrically conductive*". That is, the Examiner asserts that the only named "*nitride*" is "*silicon nitride*", and thus, correction of the above statement is required.

However, Applicants submit that the specification does not limit "*nitride*" to only "*silicon nitride*", as alleged by the Examiner, and the specification should not be interpreted as limiting "*nitride*" to only "*silicon nitride*". Instead, the specification merely states, with reference to the illustrated aspects of Figures 2-4, that the exemplary "*nitride barrier 130 is preferably silicon nitride*" (see specification at page 8, lines 1-2; emphasis added). Also, the specification merely states that "*a nitride barrier is known to be electrically conductive*" (see specification at page 6, lines 18-19; emphasis added; see also page 8, lines 21-24), not a "*silicon nitride*" barrier.

Thus, Applicants have not limited "*nitride*" to "*silicon nitride*", and therefore, no correction is believed to be required. Also, it is not believed to be necessary to list every

"*nitride*" since the ordinarily skilled artisan would know and understand the meaning of a "*nitride barrier*", and the preferred aspect which includes a "*silicon nitride barrier*".

For the foregoing reasons, Applicants submit that correction of the specification is not required. The Examiner respectfully is requested to withdraw this objection.

B. The Examiner objects to the specification as allegedly not being enabled for claim 27, since claim 27 recites that "the silicon-containing layer sets the polysilicon grain size" and the specification states that "the grain size can be different..." (see specification at page 8, lines 14-17.

Applicants note, however, that the specification clearly explains, with reference to the exemplary aspects of the invention, that the silicon-containing layer a-Si will convert to polysilicon with about 10-20 nm grain size (e.g., see Figure 2, reference numeral 125 which illustrates the small grain (about 10-20 nm grain size) polysilicon layer; e.g., the first polysilicon layer).

Then, as illustrated in Figure 3, the remaining needed polysilicon 140 (e.g., the second polysilicon layer) is deposited on the nitride barrier. The grain size of the polysilicon layer 140 (e.g., the second polysilicon layer), however, can be different (e.g., typically within a range of about 30 nm to about 80 nm), while the polysilicon layer 125 retains its small grain size because of the ultra-thin nitride barrier.

The specification further notes that there is no limit to the thickness of the polysilicon 140 (e.g., the second polysilicon layer) which is deposited, but typically it is within a range of about 80 nm to about 130 nm. The typical gate stack generally has a height (thickness) of about

100-150 nm (e.g., see specification at page 4, lines 21-24; page 6, lines 14-15; and page 8, lines 11-24).

Thus, Applicants submit that, when read in the context of the surrounding text, this portion of the specification clearly is enabling for the features of claim 27.

For the foregoing reasons, Applicants submit that correction of the specification is not required. The Examiner respectfully is requested to withdraw this objection.

V. CONCLUSION

In view of the foregoing, Applicant submits that claims 1-37, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: July 19, 2005

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CERTIFICATE OF TRANSMISSION

I certify that I transmitted via facsimile to (571) 273-8300 the enclosed Amendment under 37 C.F.R. § 1.111 to Examiner Evan T. Pert, Art Unit 2826 on July 19, 2005.

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